Carrier Transport Mechanisms of a-GaAs/ n-Si Heterojunctions

N.I.Aly, A.A.Akl, A.A.Ibrahim, and A.S.Riad

Department of Physics, Faculty of Science,
Minia University, Minia, Egypt.

Heterojunctions have been fabricated of p-type amorphous gallium arsenide (a-GaAs) thin films onto n-type silicon (n-Si) single crystals using thermal evaporation method. Current density-voltage and capacitance–voltage measurements have been performed to determine the electrical properties of the structures. Rectifying current involves tunneling and is explained by a multi-tunneling capture-emission model. The reverse current is limited by the carrier generation process. The capacitance-voltage behavior indicates an abrupt interface with a main-band discontinuity of 0.25 eV occurs in the valance band.

.

Introduction:

Amorphous III-V semiconductors and GaAs in particular, seam to be useful as optoelectronic devices working in the visible wavelength region [1]. However, little interest is being shown towards amorphous III-V semiconductors. This is presumably due to the fact that the physics of these materials is not yet completely understood. However, the realization of electronic devices using a-GaAs requires film deposition on conductive substrates which are polycrystalline (metals) or monocrystalline (semiconductors). The study of the obtained heterojunctions can be useful in obtaining an insight into amorphous- crystalline (a/c) junction properties in order to improve heterojunction devices. In addition, a-GaAs films grown on Si substrates have great interest because of their applicability to various kind of devices such as field-effect transistors [2], lasers [3] and solar cells [4].

In the present work, an a-GaAs/n-Si heterojunction was fabricated by deposition of a-GaAs (p-type) thin films as a window using the thermal evaporation method onto n-type Si single crystals. The dependence of the current density- voltage (J-V) characteristics on the temperature in both forward and reverse bias was studied in an attempt to obtain information on the transport mechanisms of the devices. In addition, capacitance-voltage (C-V) measurements were applied for characterization of these heterojunction cells. From these measurements, one can better recognize the barrier region which is formed at the interface.

Experimental:

The n-type Si<100> single crystals of resistivity 2-4 Ω cm were used as substrates. Chemical etching of n-Si was performed with $HF/NH_4F/H_2o$ (2:7:1) composition for 1.5 min, which removed effectively the surface film of silicon dioxide, SiO_2 [5]. After etching the silicon wafers were washed for 2 min in pure alcohol and distilled water. Thin films of amorphous GaAs of about 510 nm thick were deposited onto n-Si by thermal evaporation at pressure below 10^{-5} torr. X-ray diffraction (XRD) revealed that the GaAs films at substrate temperature of $\cong$ 400K are stoichometric and amorphous as well as the type of conductivity (p-type) does not change. In order to fabricate a simple heterojunction diode, an ohmic contact was preformed on the side of n-Si wafer by evaporating an indium (In) electrode. An ohmic aluminuim (Al) electrode of $\cong$ 20 nm thick was evaporated on the deposited a-GaAs films with an area of $\cong$ 1cm^2. The forward bias corresponds to the a-GaAs being positive. The current flowing through the cell was determined using a stabilized power supply and a Keithley 614 electrometer. The temperature was measured directly by means of NiCr/Ni-Al thermocouple mounted in close proximity to the cell of interest and

connected to a Keithley 871 digital thermometer. The C-V measurements were performed at room temperature using a LCR meter (Stanford Research System, model SR720) at a frequency of 1-MHz.

Results and discussion
1. Current-voltage characteristics

Fig.1 illustrates the J-V characteristics of a-GaAs/n-Si heterojunction cell at different temperatures ranging from 293 to 375 K. These curves were definitely of the diode type, with the forward direction corresponding to the positive potential on a-GaAs. This behavior can be understood by p-n junction, namely the barrier at the interface limits forward and reverse carrier flow across the junction, where the built-in potential could be developed. The rectifying ratio at 1 V for all the investigated devices was found to be in the range of 50-70 at 293 K. The gradient of the forward current, shown in Fig.2, is almost found to be constant at low voltage levels (V≤ 0.4 V). Thus, the voltage dependence of the junction current can be expressed as [6,7]:
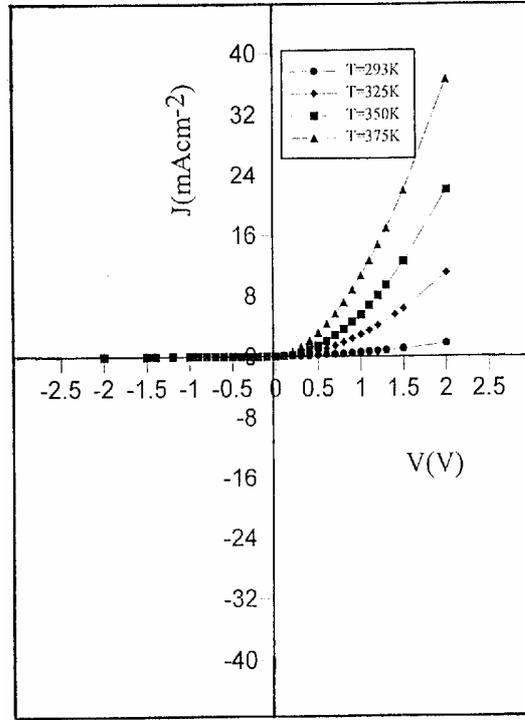
Fig.(1) J-V characteristics of a-GaAs/n-Si heterojunction at different temperatures in both forward and reverse bias.

$$J = J_0 \exp [A (V-iR_s)] \qquad (1)$$

where A is constant independent of temperature, R_s the series resistance and J_0 the reverse-saturated current density. These results suggest that the forward current under relatively low voltages are mainly dominated by multi-tunneling process [1,7]. Accordingly, J_o should change exponentially with temperature. On the other hand, the pre-exponential factor, J_0, obtained by extrapolating the forward current curves shown in Fig.2 to zero voltage, is found to vary exponentially with -1/T as shown in Fig.3 according to the relation [8,9]:

$$J0 \propto \exp (-\Delta Eaf / kT) \qquad (2)$$
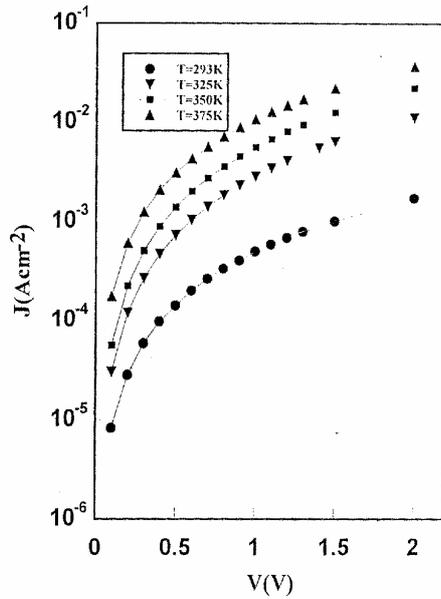
Fig.(2) Semilogarithmic plot of forward bias of J-V curves for an a-GaAs/n-Si heterojunction cell at different temperatures.
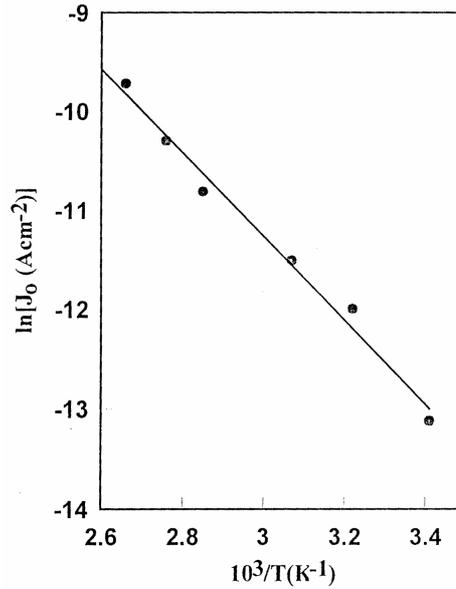
Fig.(3) Temperature dependence of the extrapolated values of J_0 obtained from Fig.2 in the forward bias.

where $\Delta E_{af} \cong 0.36$ eV is the activation energy of the charge carriers in the forward bias, which did not change exponentially with T. However, this inconsistency could be solved by considering the multi-tunneling capture-emission (MTCE) process [10] instead of multi-tunneling model. According to this process, an electron in the conduction band of n-Si flows from one localized state to another in a-GaAs located within an energy range of kT by a multi-step tunneling process. The electron keeps flowing near the edge of the depletion region of a-GaAs where the tunneling rate decreases due to a decrease of the electric filed. This electron is then either recombined with a hole in the valance band of a-GaAs, or is emitted to the conduction band of a-GaAs. This multi-tunneling process leads to the voltage dependence in eqn.(1), whereas the temperature dependence in eqn.(2) arises from either the recombination or emission process of the tunneling electron. When the MTCE model is modified by replacing the holes with the electrons for the a-GaAs/n-Si heterojunction, J_0 is described as [7]:

$$J_0 = B \ \{ \ \sigma_n \, v_{th} \, N_c \, \exp \, [- \, (E_c - E_t)/kT]$$

$$+ \sigma_p \, v_{th} \, N_v \exp[-(E_F - E_v)/kT]\} \qquad (3)$$
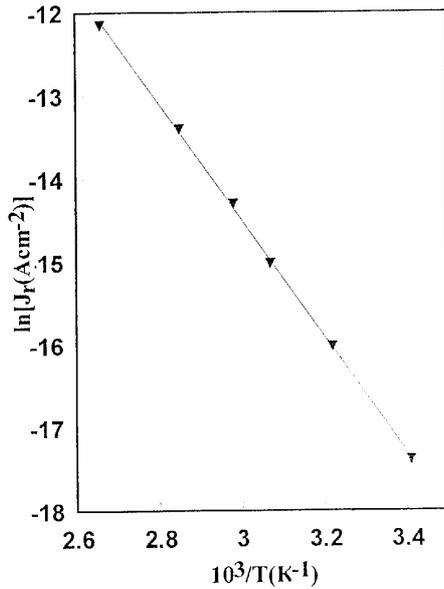
Fig.(4) Temperature dependence of the reverse current density at 0.2 V in the reverse bias.
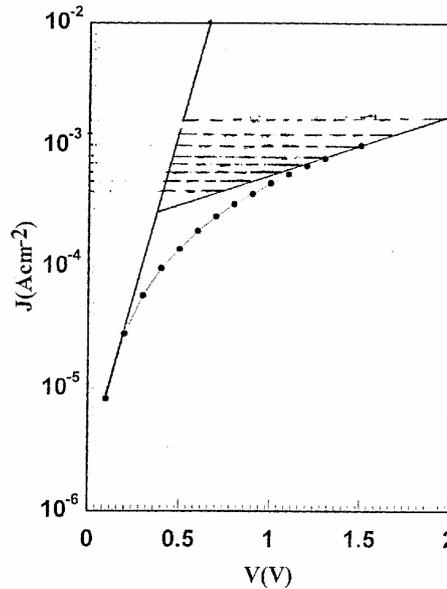
Fig.(5) Forward J-V characteristic at 293 K showing the Effect of the series resistance.

where B is constant independent of the applied voltage and temperature, σ_n the capture cross-section of the electron, v_{th} the thermal velocity, σ_p the capture cross-section of holes, N_c and N_v the effective densities of states in the conduction band and valance band of a-GaAs, respectively, and E_F, E_t, E_v and E_c the energies of the Fermi level, the trapping level, the valance band and the conduction band of a-GaAs, respectively. The first term of eqn.(3) shows an electron emission rate and the second term shows a hole capture rate. The activation energy $(E_F - E_v) = 0.62$ eV, which is obtained from the dark conductivity measurements of a-GaAs, is found to be different from the activation energy $E_{af} = 0.36$ eV obtained from Fig.3. This suggests that the electron emission process dominates the carrier transport mechanism [7,10]. Therefore, the magnitude of J_0 can be definitely determined by the first term of eqn.(3).On the other hand, the dependence of the reverse-current density J_r, on -1/T shown in Fig.4 at 0.2 V leads to the value of the activation energy $\Delta E_{ar} = 0.59$ eV of the reverse current, which is different from the obtained value of E_{af} for the forward bias. This indicates that the reverse current should be limited by the carrier generation process.

The value of the series resistance(R_s)for the cell can be determined from the forward J-V characteristics at high bias.

A Semilogarithmic plot of the forward current density versus applied voltage at 293 K is shown in Fig.5. Thus, for a given current density, J, the linear part gives the voltage drop, $\Delta V = IR_s$, across the neutral region. The plot of ΔV versus J shown in Fig.6 should give a straight line whose slope yields the value $R_s = 1.1$ kΩ.
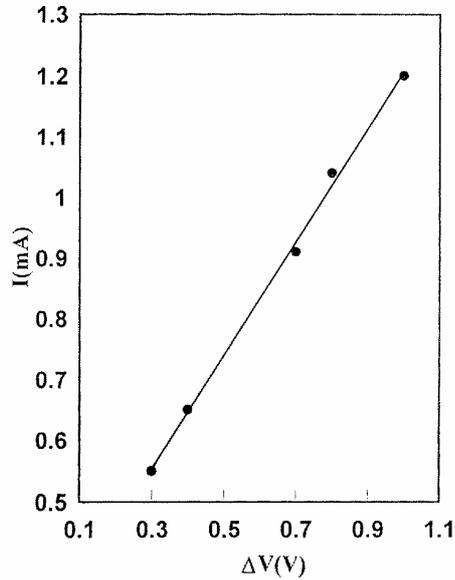
Fig.(6) The voltage drop across the series resistance, $\Delta V = IR_s$, as deduced from Fig.5.
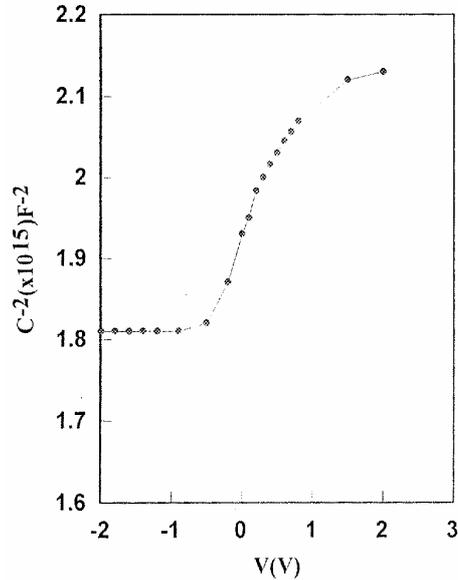
Fig.(7) Plot of C^{-2} vs. V for an a-GaAs/n-Si heterojunction in both forward and reverse bias.

2. Capacitance-voltage characteristics

Fig.7 shows the C^{-2}–V characteristic of a-GaAs/n-Si heterojunction, which is reasonably interpreted by assuming an abrupt heterojunction. This characteristic could be discussed in terms of the p-n junction type analysis [11,12,13], which the quasi-Fermi level for electrons is separated from that for holes in the depletion region when a voltage is applied across the junction, i.e. a net current flows across the a-GaAs/n-Si heterojunction.

The capacitance was measured using a small a.c. voltage of 1-MHz. The resistivity, ρ_1, of n-Si used in this study was found to be lower than 10 Ωcm, so that the dielectric relaxation time ($\rho_1\varepsilon^{\backslash}_1$, where $\varepsilon^{\backslash}_1$ is the permmitivity of Si) became 10^{-11} s, which indicated that the redistribution of electrons (majority carriers of n-Si) can respond to the 1-MHz a.c. voltage. On the other hand, the minimum value of resistivity, ρ_2, for the a-GaAs films was 10^7 Ωcm. Therefore, the dielectric relaxation time became 10^{-5}s, which suggested that the

redistribution of holes (majority carriers of a-GaAs) can not respond to an a.c. voltage higher than 100 kHz. Thus, the films may be considered as a dielectric material in its behavior in the case of the 1-MHz a.c. voltage. This indicated that the capacitance of a- GaAs film equals to its geometric capacitance due to its longer dielectric relaxation time. Since the capacitance of a-GaAs films measured at 1-MHz showed a constant value of $\cong$ 23.5 nF, independent of the applied voltage as shown in Fig.7, one can obtain information on the depletion layer extending in the n-Si side regardless of that of a-GaAs side. Therefore, the total capacitance, C, of the junction can be expressed by the relation[1,14]:

$$1/C = 1/C_1 + 1/C_2 = (1/S\varepsilon_0) \left[(\omega_1 / \varepsilon_1) + (t / \varepsilon_2) \right] \qquad (4)$$

where C_1, ω_1 and ε_1 are, respectively, the capacitance, the width of the depletion region in the n-Si side and the dielectric constant of n-Si, i.e. 11.8, S the effective area of the cell, and t, ε_2, and C_2 are, respectively, the thickness, the dielectric constant, 13.33, and the capacitance of the a-GaAs films which should be given by :

$$C2 = \varepsilon o \, \varepsilon 2 \, S / t \qquad (5)$$

According to the abrupt heterojunction model [5,11], the following two relations:

$$(VD1 - V1) / (VD2 - V2) = N2 \, \varepsilon 2 / N1 \, \varepsilon 1 \qquad (6)$$

and

$$\omega 1 = 2 \, \varepsilon 1 \, \varepsilon 0 \, (VD1 - V1) / q \, N1 \qquad (7)$$

are easily derived, where V_1 and V_2 are the d.c. bias being supported in the depletion region in n-Si and a-GaAs, respectively, N_2 is the effective density of localized gap states in a-GaAs, N_1 is the donor concentration in the n-Si, 1.2×10^{15} cm^{-3}, which was determined by C-V measurements on Al/n-Si Schottky-barrier diode. Eqn.(6)can be rewritten in the following form:

$$(V_{D1} - V_1) / (V_D - V) = N_2 \varepsilon_2 / (N_1 \varepsilon_1 + N_2 \varepsilon_2) \qquad (8)$$

where $V = V_1 + V_2$ is the total applied voltage through the heterojunction. From eqns. (4), (7) and (8), the following relations could be easily derived as:

$$\omega^2_1 = \{ \varepsilon_o \, \varepsilon_1 \, S \, [(1/C) - (1/C_2)] \}^2 \qquad (9)$$
$$= [2 \, \varepsilon_o \, \varepsilon_2 \varepsilon_1 \, N_2 \, (V_D - V)] / [q \, N_1 \, (N_1 \, \varepsilon_1 + N_2 \, \varepsilon_2)] \qquad (10)$$

where $V_D = V_{D1} + V_{D2}$ is the total built-in voltage.

Fig.8 shows the plot of ω^2_1 versus V calculated from the data of Fig.7 with eqn.(9). The saturated capacitance value, C_2, of 23.5 nF with the forward bias has been used to calculate ω_1 in eqn.(9). This plot reveals a good linear relationship indicating that the abrupt heterojunction model is applicable to the a-GaAs/n-Si structure. It is clear from eqn.(10) that the values of N_2 and V_D are graphically determined from the slope of the curve shown in Fig.8 and the intercept on the horizontal axis; their values were found to be $=1.03 \times 10^{16}$ cm^{-3}, and 0.31 eV, respectively. The obtained value of N_2 almost coincides (within the experimental error) with the value of 1.05×10^{16} cm^{-3}, determined from C-V measurements on the In/a-GaAs Schottky diode.
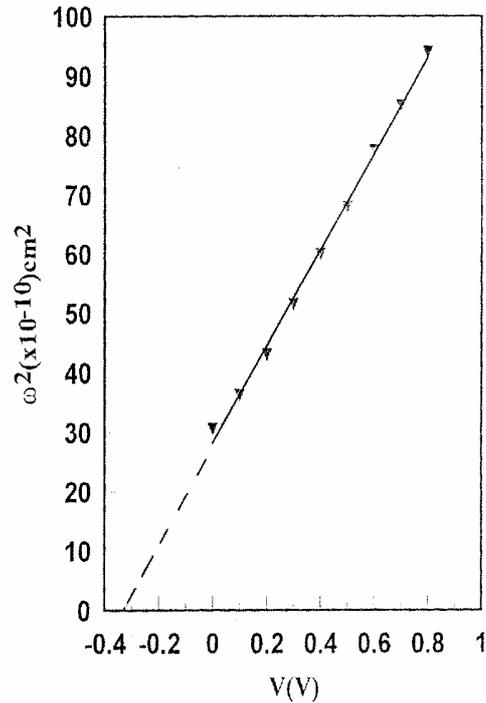
Fig.(8) Width of the depletion region in n-Si as a function of voltage.

3. Energy-band diagram of a-GaAs/n-Si heterojunction

Anderson [15] has initially proposed an energy-band diagram assuming no interface states and extremely abrupt change from one material to the other. Since the energy gaps of the two semiconductors are different, there must be a discontinuity in one or both edges at the interface. The conduction band discontinuity, ΔE_c, is expressed by [5,11]:

$$\Delta E_c = \delta_1 + \delta_2 - E_{g1} + qV_D \qquad (11)$$

where $\delta_2 (= E_F - E_V)$, is considered to be activation energy of a-GaAs, 0.61 eV, $\delta_1 [= kT \ln (N_c / N_1)$,where N_c is the effective denisty of states for n-Si] is the position of the Fermi level for n-Si from the bottom of the conduction band, (0.23 eV for $N_1 = 1.2 \times 10^{15}$ cm^{-3}, and $N_c = 1.02 \times 10^{19} cm^{-3}$ [10]), and E_{g1} is the energy bandgap of n-Si, 1.12 eV [5].

A value of ΔE_c was then calculated and found to be 0.03 eV. Taking the value of the energy bandgap of a-GaAs, $\Delta E_{g2} = 1.4$ eV [1], and using the well-known formula :

$$\Delta E_c + \Delta E_V = E_{g2} - E_{g1} \qquad (12)$$

The valence band offset, ΔE_V, was then estimated and found to be 0.25 eV, indicating that the main-band discontinuity occurs in the valance band. A schematic band model of the a-GaAs / n-Si interface is shown in Fig.9.
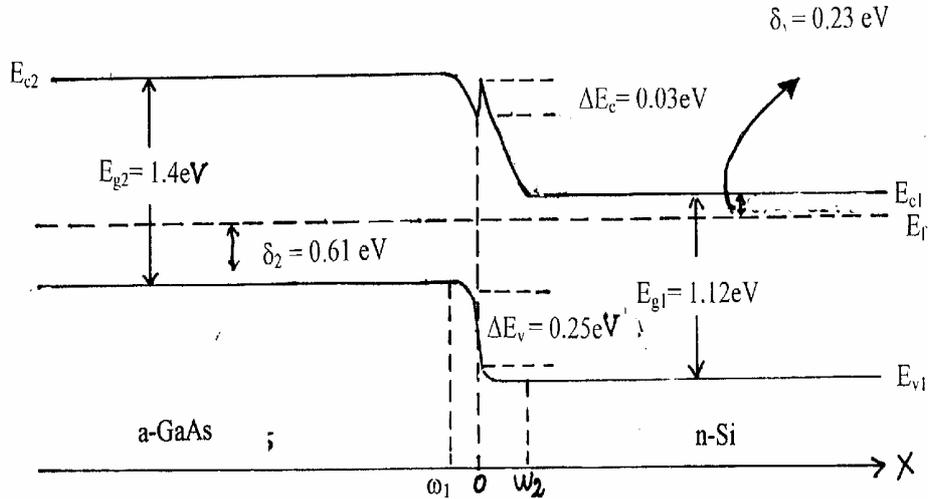
Fig.(9) Energy-band diagram in the interface region for an a-GaAs/n-Siheterojunction at equilibrium.

Summary and conclusions

Heterojunction devices of a-GaAs onto n-Si <100> substrates have been fabricated by thermal evaporation method. These junctions exhibit rectifying characteristics showing a p-n diode-like behavior. The dark current-voltage measurements suggest that the forward current in these junctions involves tunneling and is explained by a multi-tunneling capture-emission model in which the electron emission process dominates the carrier transport mechanism. On the other hand, the reverse current may be reasonably ascribed to a generated current. The series resistance and activation energy of the charge carriers have been obtained by analyzing the dark current-voltage characteristics. From the capacitance-voltage measurements at high frequency of 1-MHz, one can obtain information on the depletion layer extending in the Si side regardless of that in the GaAs side. These characteristics are reasonably interpreted by assuming an ideal abrupt heterojunction. An energy band diagram is proposed in which the main-band discontinuity occurs in the valance band.

References:

1. K. Aguir, A. Fennouh, H. Carchano, J. Lseguin, B. Elhadadi and F.Lalande, Thin Solid Films **257**, 98 (1995).
2. T. Nakanishi, T.Vdagawa, A. Tanaka and K. Kamei, J. Cryst. Growth **55**, 4578 (1985).
3. S. Sakai, T. Soga, M. Takeyasu, and M. Umeno, Appl. Phys. Lett. **48**, 413 (1986).
4. R.P. gale, J.C.C. Fan, B.Y Tasur, G.W.Turner, and F.M. Davis, TEEE Electron Device leh EDL-2, **169**(1981); Y. Itoh, T. Nishioka, A. Yamamoto, and M. Yamagucw. Appl. Phys. Lett. **49**, 1614 (1986).
5. S. Darwish, A.S. Riad and H.S. Soliman, Semicond. Sci. Technol. **11**, 96 (1995).
6. M. Igalson, phys. status solidi **A124**, K15 (1991).
7. H. Mimura, Y. Hatanaka, J. Appl. Phys. **71**, 2315 (1992).
8. S. K. Das and G. C. Morris, Sol. Energ. Mat. Sol. **C.28**, 305 (1993).
9. A. S. Riad, Thin Solid Films **370**, 253 (2000).
10. H. Matsuara, T. Okuno, H-Okushi and K. Tanaka, J. Appl. Phys. **55**, 1012 (1984).
11. H. Matsuura, J. Appl. Phys. 64(1988)1964.
12. A.S.Riad, R.M. Abdel-Latif and S.Darwish, Egypt. J. Sol. **22**, 231 (1999).
13. S. Darwish, H.S. Soliman and A.S.Riad, Thin Solid Films **259**, 248 (1995).
14. A.S. Riad, S. Darwish and H.H. Afify, Thin Solid Films **391**, 109 (2001).
15. R.L.Andorson, Solid-State Electron, **5**, 341 (1962).